

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT  (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. DATUMTE.018A	APPLICATION NO. unknown 10820381
	APPLICANT Plasterer, et al.	
	FILING DATE Herewith	GROUP Unknown

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)	
A1	6525571		Green				
	6501314		Ling				
	6424194		Hairapetian				
	6340899		Green				
	6320422		Koh				
	6028454		Elmasry et al.				
	6014041		Somasekhar et al.				
	5945858		Sato				
	5892382		Ueda et al.				
	5877642		Takahashi				
	5726613		Hayashi et al.				
	5216295		Hoang				
	5202655		Hara				
	4333020		Maerder				
	2003-0122603 A1		Green				

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
A1	Allam, M, et al., "Dynamic Current Mode Logic (DyCML): A New Low-Power High-Performance Logic Style," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 36, No. 3, (March 2001), Institute of Electrical and Electronics Engineers, Inc., pp. 550-558.
	Hara, S., et al., "Broad-band Monolithic Microwave Active Inductor and Its Application to Miniaturized Wide-Band Amplifiers," <i>IEEE Transactions on Microwave Theory and Techniques</i> , Vol. MTT-36, No. 12, (Dec. 1998) Institute of Electrical and Electronics Engineers, Inc., pp. 1920-1924.
	Kiaei, S., et al., "CMOS Source-Coupled Logic for Mixed-Mode VLSI," <i>IEEE International Symposium on Circuits and Systems</i> (23rd: 1990: New Orleans), Institute of Electrical and Electronics Engineers, Inc., pp. 1608-1611.

EXAMINER	DATE CONSIDERED
<i>[Signature]</i>	7/22/05

\*EXAMINER: INITIAL IF CITATION CONSIDERED. WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  <b>INFORMATION DISCLOSURE STATEMENT          BY APPLICANT</b>  (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. DATUMTE.018A	APPLICATION NO. unknown 1082038/
	APPLICANT Plasterer, et al.	
	FILING DATE Herewith	GROUP Unknown

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
AT	Kundan, J., et al., "Enhanced Folded Source-Coupled Logic Technique for Low-Voltage Mixed-Signal Integrated Circuits," <i>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</i> , Vol. 47, No. 8 (Aug. 2000) Institute of Electrical and Electronics Engineers, Inc., pp. 810-817.
	Tanabe, A., et al., "0.18- $\mu$ m CMOS 10-Gb/s Multiplexer/Demultiplexer ICs Using Current Mode Logic with Tolerance to Threshold Voltage Fluctuation," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 36, No. 6 (June 2001) Institute of Electrical and Electronics Engineers, Inc., pp. 988-996.
JD	Yamashina, M, et al., "An MOS Current Mode Logic (MCML) Circuit For Low-Power Sub-Ghz Processors," <i>IEICE Transactions on Electronics</i> , Vol. E75-C (Oct. 1992), Institute of Electronics, Information and Communication Engineers, pp. 1181-1187.

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